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Method and Apparatus for Reducing Fixed Charge in Semiconductor Device Layers

This application is a Continuation of U.S. Application No. 10/228,697, filed August 26, 2002, which is a Continuation of U.S. Application No. 09/145,723, filed September 2, 1998, now U.S. Patent No. 6,441,466, which is a Divisional of U.S. Application No. 08/972,288, filed July 9, 1996, now U.S. Patent No. 5,933,760, which is a File-Wrapper Continuation of U.S. Application No. 08/594,652, filed February 2, 1996, now abandoned.

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Field of the Invention

The present invention relates to methods and apparatus for manufacturing semiconductor devices, and in particular to reducing the fixed charge in insulative layers on such devices.

Background of the Invention

Field effect transistors (FETs) are formed on silicon, or similar semiconductor substrates. A field effect transistor is usually formed with active areas such as two heavily doped, spaced apart regions of silicon, which are called a source and a drain. A gate structure is formed between the source and the drain, and operates to control the amount of electrical current which flows between them. When appropriate voltage is applied to the gate, an electrically conductive channel is formed under the gate, allowing current flow between the source and the drain. Active areas of adjacent transistors may be isolated from each other by the formation of a field oxide layer which acts as an insulator.

Part of the process of forming transistors involves the application of various layers of material. One such layer is utilized as an insulating layer between the gate and metal interconnects. Silane based layers have been used in the past, but do not fill tight spaces very well. Tetraethyloxysilicate (TEOS) based borophosphosilicate glass (BPSG) film layers using TEOS is a silicon containing